Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **PHASE COMP PULSEOUT**
2. **PHASE COMP 1 OUT**
3. **COMP IN**
4. **VCO OUT**
5. **INHIBIT IN**
6. **C1A**
7. **C1B**
8. **GND**
9. **VCO IN**
10. **DEMODULATOR OUT**
11. **R1**
12. **R2**
13. **PHASE COMP 2 OUT**
14. **SIGNAL IN**
15. **PHASE COMP 3 OUT**
16. **VCC**

**6 5 4 3**

**2**

**1**

**16**

**15**

**K74A**

**HC4046 L**

**MASK**

**REF**

**7**

**8**

**9**

**10**

**11 12 13 14**

**.062”**

**.068”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .005” X .005”**

**Backside Potential:**

**Mask Ref: HC4046 L**

**APPROVED BY: DK DIE SIZE .062” X .068” DATE: 4/29/16**

**MFG: ON-SEMI THICKNESS .012” P/N: 54HC4046A**

**DG 10.1.2**

#### Rev B, 7/1